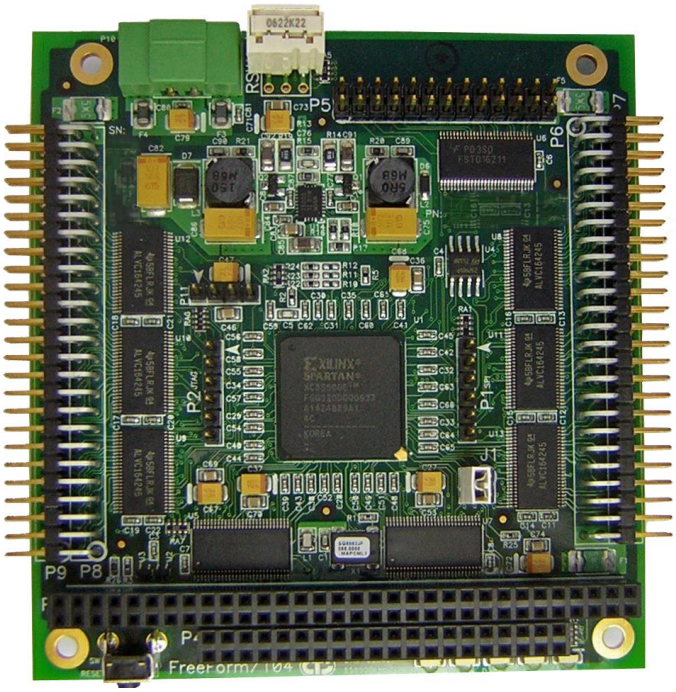
Connect Tech Inc.

FreeForm/104

PC/104 Reconfigurable Digital I/O with Counter/Timers
User's Manual



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CTIM-00036 Revision 0.04 July 21, 2011

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Introduction

Connect Tech's FreeForm/104 is a PC/104 bus based assembly featuring a Xilinx Spartan 3E FPGA for reconfigurable computing. The FreeForm/104 offers users off-the-shelf functionality for standard digital I/O and counter/timer applications or the option to develop custom FPGA configurations.

Features

Board Description

- Customizable PC/104 based board featuring a Xilinx Spartan 3E FPGA – 500,000 gates, 360K RAM
- FPGA configurable through persistent storage in SPI Flash (4Mb) or over JTAG for development and debugging
- 66MHz internally scaleable input clock
- External 5V power connection for stand alone usage
- Four user LEDs and eight position rotary switch connected to FPGA
- On-board reset switch
- Fixed I/O – 12 inputs, six bi-directional 5V TTL.
- Programmable I/O - 96 bi-directional 5V high current (+/-24mA) TTL/CMOS
- Commercial temperature range

Standard Digital I/O and Counter/Timer Configuration

The standard configuration for FreeForm/104 consists of:

- PC/104: eight bit I/O slave with a 32 byte address space - base address is selectable via rotary switch
- Digital I/O: 4 x 8255 compatible blocks, uses programmable I/O
- Counter/timers: 2 x 8254 compatible block, uses fixed I/O - optional internal clock source selection
- User status LEDs

Custom Configurations

FreeForm/104 custom configurations can be developed making use of the following interfaces and I/O connected to the FPGA:

- PC/104 Interfaces: eight data lines, 12 address lines, all IRQs, and DMA Channels zero to three
- Programmable I/O
- Fixed I/O
- LEDs
- Rotary switch
- SPI flash for parameter storage

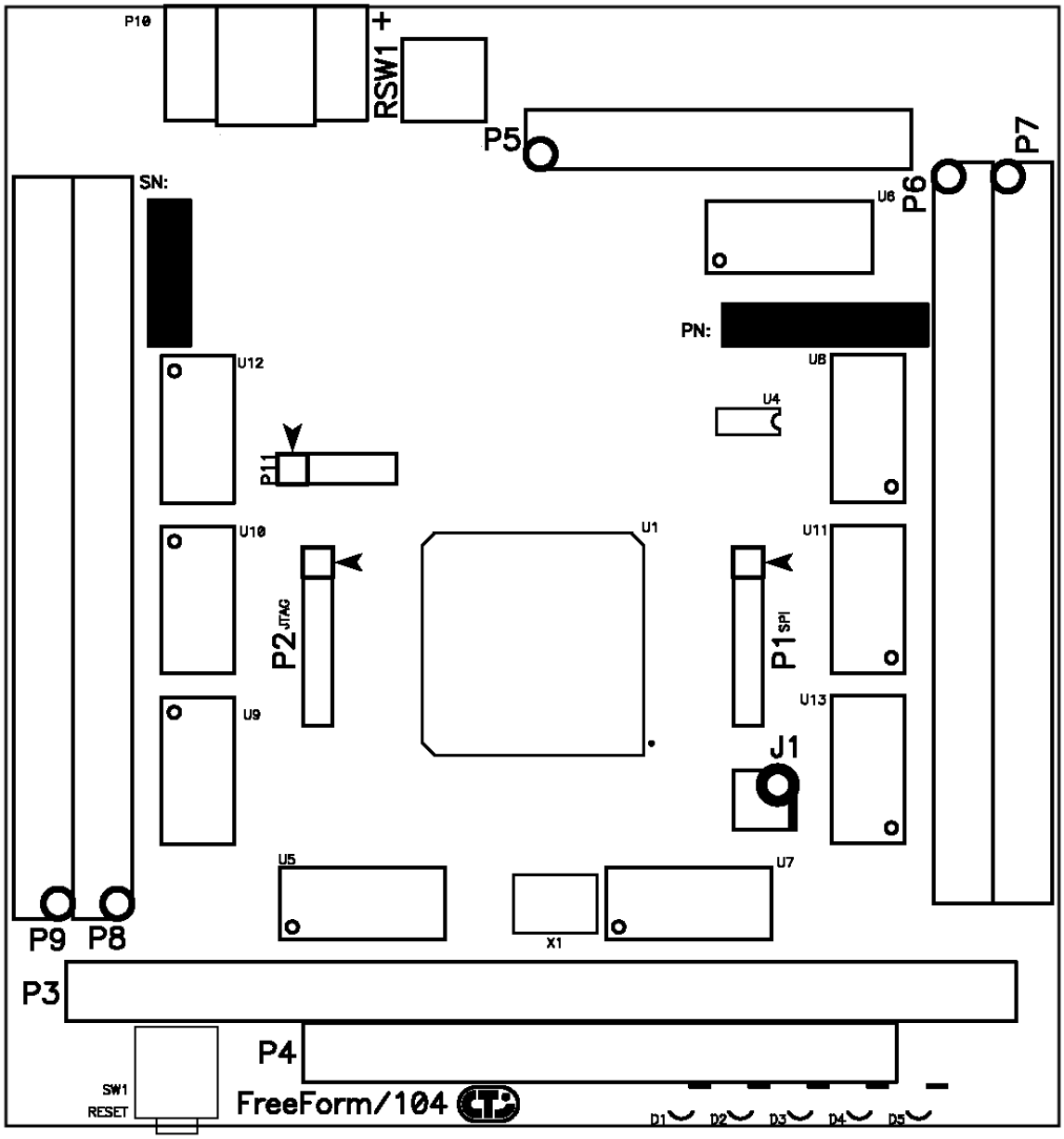

Figure 1: FreeForm/104 Layout

Table 1: FreeForm/104 Components

Connectors	Description
P1	SPI Programming
P2	JTAG Programming
P3,P4	PC/104
P5	Counter/timer
P6,P8	Digital I/O
P7,P9	Digital I/O, Opto-22 compatible
P10	5V+ Input
P11	Voltage reference
Jumpers /Switches	**Description**
RSW1	Address selection rotary switch
J1	FPGA configuration selection
SW1	Reset push button
Components	**Description**
D1	FPGA OK LED
D2-D5	User LEDs
U1	Xilinx FPGA
U5-U7	Isolation switches
U8-U13	High current buffers
X1	Oscillator

NOTE: If the board is the Opto-22 compatible model, then connectors P7 and P9 will be populated.

Hardware Description and Configuration

The following sections describe the functions of all switches/jumpers and provide details on connector pin-outs.

Jumpers and Switches

Base Address Selection (RSW1)

This rotary switch selects a base address in the PC/104 I/O address space. Note that the rotary switch input is only sampled during the board initialization phase; therefore any selections made will not take effect until the next reset or power cycle.

FreeForm/104 requires 32 bytes of I/O memory. Refer to the I/O Register Map for details.

Table 2: Base Address Selection (RSW1)

Rotary Switch Position	Base Address
0	300
1	320
2	340
3	360
4	380
5	3A0
6	3C0
7	3E0

NOTE: Custom addressing schemes are available upon request. Contact Connect Tech for more information.

FPGA Configuration Settings (J1)

Jumper J1 is used to control FPGA configuration.

Table 3: FPGA Configuration Settings (J1)

Pins	Function	
1-2	On	Hold FPGA pins in tri-state, required for Flash programming
	Off	FPGA pins function as programmed
3-4	On	FPGA loads configuration from SPI Flash.
	Off	FPGA waits for configuration over JTAG

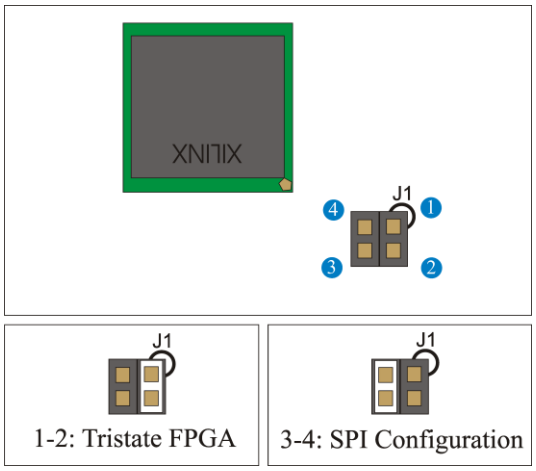

Figure 2: FPGA Configuration Settings (J1)

Settings should only be modified during user customization. Knowledge of FPGA internals and programming are required before attempting any user customization. See the FreeForm/104 configuration manual for details.

Reset Switch (RSW1)

Pushing the reset switch initiates the FPGA programming cycle causing the FPGA to reload its configuration. Once the FPGA configuration has loaded successfully, the FPGA OK LED (D1) will turn on.

During the programming cycle, the FreeForm/104 disconnects from all I/O – including the PC/104 connector.

Connector Pin-outs

Table 4: SPI Flash Programming Header (P1)

Pin	Signal	Direction
1	SPI_SS#	input
2	SPI_MOSI	input
3	SPI_MISO	output
4	SPI_SCLK	input
5	GND	signal ground
6	+3.3V	reference

Table 5: JTAG Programming Header (P2)

Pin	Signal	Direction
1	TMS	input
2	TDI	input
3	TDO	output
4	TCK	input
5	GND	signal ground
6	+3.3V	reference

Table 6: PC/104 Connector (P3, P4)

Refer to PC/104 specifications, available from the PC/104 Consortium website at http://www.pc104.org/.

Table 7: Counter/Timer Header (P5)

Pin	Signal	Direction
1	TC_0CLK	input
2	TC_0GATE	input
3	TC_0OUT	output
4	GND	signal ground
5	TC_1CLK	input
6	TC_1GATE	input
7	TC_1OUT	output
8	GND	signal ground
9	TC_2CLK	input
10	TC_2GATE	input
11	TC_2OUT	output
12	GND	signal ground
13	TC_3CLK	input
14	TC_3GATE	input
15	TC_3OUT	output
16	GND	signal ground
17	TC_4CLK	input
18	TC_4GATE	input
19	TC_4OUT	output
20	GND	signal ground
21	TC_5CLK	input
22	TC_5GATE	input
23	TC_5OUT	output
24	GND	signal ground
25	+5V	power
26	+5V	power

Table 8: Digital I/O Headers (P6, P8)

Pin	Digital I/O (P6)		Opto-22 Digital I/O (P7)	
	Signal	**Direction**	**Signal**	**Direction**
1	DIO_0A7	input/output	DIO_0A7	input/output
2	DIO_1A7	input/output	GND	signal ground
3	DIO_0A6	input/output	DIO_0A6	input/output
4	DIO_1A6	input/output	GND	signal ground
5	DIO_0A5	input/output	DIO_0A5	input/output
6	DIO_1A5	input/output	GND	signal ground
7	DIO_0A4	input/output	DIO_0A4	input/output
8	DIO_1A4	input/output	GND	signal ground
9	DIO_0A3	input/output	DIO_0A3	input/output
10	DIO_1A3	input/output	GND	signal ground
11	DIO_0A2	input/output	DIO_0A2	input/output
12	DIO_1A2	input/output	GND	signal ground
13	DIO_0A1	input/output	DIO_0A1	input/output
14	DIO_1A1	input/output	GND	signal ground
15	DIO_0A0	input/output	DIO_0A0	input/output
16	DIO_1A0	input/output	GND	signal ground
17	DIO_0B7	input/output	DIO_0B7	input/output
18	DIO_1B7	input/output	GND	signal ground
19	DIO_0B6	input/output	DIO_0B6	input/output
20	DIO_1B6	input/output	GND	signal ground
21	DIO_0B5	input/output	DIO_0B5	input/output
22	DIO_1B5	input/output	GND	signal ground
23	DIO_0B4	input/output	DIO_0B4	input/output
24	DIO_1B4	input/output	GND	signal ground
25	DIO_0B3	input/output	DIO_0B3	input/output
26	DIO_1B3	input/output	GND	signal ground
27	DIO_0B2	input/output	DIO_0B2	input/output
28	DIO_1B2	input/output	GND	signal ground
29	DIO_0B1	input/output	DIO_0B1	input/output
30	DIO_1B1	input/output	GND	signal ground
31	DIO_0B0	input/output	DIO_0B0	input/output
32	DIO_1B0	input/output	GND	signal ground
33	DIO_0C7	input/output	DIO_0C7	input/output
34	DIO_1C7	input/output	GND	signal ground
35	DIO_0C6	input/output	DIO_0C6	input/output
36	DIO_1C6	input/output	GND	signal ground
37	DIO_0C5	input/output	DIO_0C5	input/output
38	DIO_1C5	input/output	GND	signal ground
39	DIO_0C4	input/output	DIO_0C4	input/output
40	DIO_1C4	input/output	GND	signal ground
41	DIO_0C3	input/output	DIO_0C3	input/output
42	DIO_1C3	input/output	GND	signal ground
43	DIO_0C2	input/output	DIO_0C2	input/output
44	DIO_1C2	input/output	GND	signal ground
45	DIO_0C1	input/output	DIO_0C1	input/output
46	DIO_1C1	input/output	GND	signal ground
47	DIO_0C0	input/output	DIO_0C0	input/output
48	DIO_1C0	input/output	GND	signal ground
49	+5V	power	+5V	power
50	GND	power	GND	power

Table 9: Digital I/O Headers (P7, P9)

Pin	Digital I/O (P8)		Opto-22 Digital I/0 (P9)	
	Signal	**Direction**	**Signal**	**Direction**
1	DIO_2A7	input/output	DIO_2A7	input/output
2	DIO_3A7	input/output	GND	signal ground
3	DIO_2A6	input/output	DIO_2A6	input/output
4	DIO_3A6	input/output	GND	signal ground
5	DIO_2A5	input/output	DIO_2A5	input/output
6	DIO_3A5	input/output	GND	signal ground
7	DIO_2A4	input/output	DIO_2A4	input/output
8	DIO_3A4	input/output	GND	signal ground
9	DIO_2A3	input/output	DIO_2A3	input/output
10	DIO_3A3	input/output	GND	signal ground
11	DIO_2A2	input/output	DIO_2A2	input/output
12	DIO_3A2	input/output	GND	signal ground
13	DIO_2A1	input/output	DIO_2A1	input/output
14	DIO_3A1	input/output	GND	signal ground
15	DIO_2A0	input/output	DIO_2A0	input/output
16	DIO_3A0	input/output	GND	signal ground
17	DIO_2B7	input/output	DIO_2B7	input/output
18	DIO_3B7	input/output	GND	signal ground
19	DIO_2B6	input/output	DIO_2B6	input/output
20	DIO_3B6	input/output	GND	signal ground
21	DIO_2B5	input/output	DIO_2B5	input/output
22	DIO_3B5	input/output	GND	signal ground
23	DIO_2B4	input/output	DIO_2B4	input/output
24	DIO_3B4	input/output	GND	signal ground
25	DIO_2B3	input/output	DIO_2B3	input/output
26	DIO_3B3	input/output	GND	signal ground
27	DIO_2B2	input/output	DIO_2B2	input/output
28	DIO_3B2	input/output	GND	signal ground
29	DIO_2B1	input/output	DIO_2B1	input/output
30	DIO_3B1	input/output	GND	signal ground
31	DIO_2B0	input/output	DIO_2B0	input/output
32	DIO_3B0	input/output	GND	signal ground
33	DIO_2C7	input/output	DIO_2C7	input/output
34	DIO_3C7	input/output	GND	signal ground
35	DIO_2C6	input/output	DIO_2C6	input/output
36	DIO_3C6	input/output	GND	signal ground
37	DIO_2C5	input/output	DIO_2C5	input/output
38	DIO_3C5	input/output	GND	signal ground
39	DIO_2C4	input/output	DIO_2C4	input/output
40	DIO_3C4	input/output	GND	signal ground
41	DIO_2C3	input/output	DIO_2C3	input/output
42	DIO_3C3	input/output	GND	signal ground
43	DIO_2C2	input/output	DIO_2C2	input/output
44	DIO_3C2	input/output	GND	signal ground
45	DIO_2C1	input/output	DIO_2C1	input/output
46	DIO_3C1	input/output	GND	signal ground
47	DIO_2C0	input/output	DIO_2C0	input/output
48	DIO_3C0	input/output	GND	signal ground
49	+5V	power	+5V	power
50	GND	power	GND	power

Table 10: Counter/Timer Header (P5)

Pin	Signal	Direction
1	TC_0CLK0	input
2	TC_0GATE0	input
3	TC_0OUT0	output
4	GND	signal ground
5	TC_0CLK1	input
6	TC_0GATE1	input
7	TC_0OUT1	output
8	GND	signal ground
9	TC_0CLK2	input
10	TC_0GATE2	input
11	TC_0OUT2	output
12	GND	signal ground
13	TC_1CLK0	input
14	TC_1GATE0	input
15	TC_1OUT0	output
16	GND	signal ground
17	TC_1CLK1	input
18	TC_1GATE1	input
19	TC_1OUT1	output
20	GND	signal ground
21	TC_1CLK2	input
22	TC_1GATE2	input
23	TC_1OUT2	output
24	GND	signal ground
25	+5V	power
26	+5V	power

Table 11: External Power Supply (P10)

Pin	Signal	Direction
1	+5V	power
2	GND	power

Table 12: Voltage Reference (P11)

Pin	Signal	Direction
1	+2.5V	reference
2	+1.2V	reference
3	+3.3V	reference
4	GND	reference

Hardware Installation & Configuration

Before installing the FreeForm/104 into your PC/104 stack, ensure the following:

1) PC/104 base address is properly selected using the rotary switch RSW1. Note that the FreeForm/104 address space consumes 32 bytes.
2) FPGA configuration jumper J1 is set to read from Flash
3) All cables are connected

Once installed in the system and power is applied, the LED D1 will illuminate to indicate that FreeForm/104 is functioning properly.

WARNING: Do not plug an external power cable into P10 (+5V input) while the FreeForm/104 is plugged into a PC/104 stack. This can cause contention between the system power supply and the external power supply, potentially damaging circuitry.

Programming Reference

The standard configuration for FreeForm/104 contains 4 x 8255 compatible cores and 2 x 8254 counter/timer compatible cores. Connect Tech provides drivers for several operating systems, as well as, a software development kit (SDK). The SDK encapsulates many of the standard 8254 and 8255 operations required by applications. For further information on installing the driver and the SDK refer to Software Installation.

The FreeForm/104 I/O Register Map and details on each register are provided for developers with applications that require direct access to the hardware.

Using the 8255 Digital I/O

FreeForm/104 has 96 bi-directional digital I/O lines that are controlled by 4 x 8255 blocks: DIO_0, DIO_1, DIO_2 and DIO_3. DIO_0 and DIO_1 are connected to P6/P7 while DIO_2 and DIO_3 are connected to P8/P9.

Connect Tech's FPGA implementation of the original Intel 82C55A follows its datasheet specification with the following exceptions:

- The bus interface is synchronous to the main FPGA clock
- Only Mode 0 is implemented to due to the limitations of the external hardware
- Bit set/clear through the control register is available for all ports, not port C exclusively

For more information on programming with the 8255, refer to the Intel 82C55A datasheet in the \datasheets directory on the CD.

Using the 8254 Counter/Timer

Six counter/timers are contained in 2 x 8254 compatible blocks TC_0 and TC_1. TC_0 and TC_1 gate, clock and output signals are connected to P5 on FreeForm/104.

General 8254 Counter/Timer Features:

- Three functionally equivalent counter/timers
- Each counter/timer has a register for loading and reading the current count
- A control register for programming the counting mode and read/write format
- A read/write format that is either a byte operation (LSB or MSB) or two consecutive byte operations (LSB followed by MSB)
- Six counting modes:
    - Mode 0: Interrupt on Terminal Count
    - Mode 1: Hardware Re-triggerable One-shot
    - Mode 2: Rate Generator
    - Mode 3: Square Wave
    - Mode 4: Software Triggered Strobe
    - Mode 5: Hardware Triggered Strobe
- Counters are programmed by:
    - Writing read/write format and mode to control register
    - Writing initial count to count register, either one or two bytes

Connect Tech's FPGA implementation of the original Intel 8254 follows the datasheet specification with the following exceptions:

- The bus interface is synchronous to the main FPGA clock
- The output signal is low on reset, until a control word is written
- Mode=0 and R/W=LSB/MSB: once the count hits 0 and output is set high, output does not go low until both bytes are written or a new control word is written

As an added feature, a Counter Clock Source register has been provided which can direct the counter/timers to use internal timing resources as an alternative to using the provided external clocks.

For more information on programming with the 8254, refer to the Intel 8254 datasheet in the \datasheets directory on the CD.

I/O Register Map

The following table outlines the I/O register map of the FreeForm/104. Where applicable, the associated signals are listed. Refer to the Connector pin-outs for signal to pin connectivity.

Table 13: I/O Register Map

Offset	Read/Write	Register	Associated Signals
0x00	R/W	8255 0 Port A I/O	P6/P7: DIO_0A<7..0>
0x01	R/W	8255 0 Port B I/O	P6/P7: DIO_0B<7..0>
0x02	R/W	8255 0 Port C I/O	P6/P7: DIO_0C<7..0>
0x03	R/W	8255 0 Control	
0x04	R/W	8255 1 Port A I/O	P6/P7: DIO_1A<7..0>
0x05	R/W	8255 1 Port B I/O	P6/P7: DIO_1B<7..0>
0x06	R/W	8255 1 Port C I/O	P6/P7: DIO_1C<7..0>
0x07	R/W	8255 1 Control	
0x08	R/W	8255 2 Port A I/O	P8/P9: DIO_2A<7..0>
0x09	R/W	8255 2 Port B I/O	P8/P9: DIO_2B<7..0>
0x0A	R/W	8255 2 Port C I/O	P8/P9: DIO_2C<7..0>
0x0B	R/W	8255 2 Control	
0x0C	R/W	8255 3 Port A I/O	P8/P9: DIO_3A<7..0>
0x0D	R/W	8255 3 Port B I/O	P8/P9: DIO_3B<7..0>
0x0E	R/W	8255 3 Port C I/O	P8/P9: DIO_3C<7..0>
0x0F	R/W	8255 3 Control	
0x10	R/W	8254 0 Counter 0	P5: TC_0GATE0, TC_0CLK0, TC_0OUT0
0x11	R/W	8254 0 Counter 1	P5: TC_0GATE1, TC_0CLK1, TC_0OUT1
0x12	R/W	8254 0 Counter 2	P5: TC_0GATE2, TC_0CLK2, TC_0OUT2
0x13	W	8254 0 Control	
0x14	R/W	8254 1 Counter 0	P5: TC_1GATE0, TC_1CLK0, TC_1OUT0
0x15	R/W	8254 1 Counter 1	P5: TC_1GATE1 TC_1CLK1 TC_1OUT1
0x16	R/W	8254 1 Counter 2	P5: TC_1GATE2 TC_1CLK2 TC_1OUT2
0x17	W	8254 1 Control	
0x18	R/W	Counter Clock Source	
0x19	R/W	User LEDs	D2-D5: LED<3..0>
0x1A		*reserved*	
0x1B	R/W	Revision	
0x1C		*reserved*	
0x1D		*reserved*	
0x1E		*reserved*	
0x1F		*reserved*	

Register Details

8255 Control Register

There are two different formats used when writing the control register: 1) Mode Selection and 2) Bit/Set Clear.

1) Mode Selection Format (Bit 7 = 1)
Writing to the control register using this format will change the direction of the ports.

7	6	5	4	3	2	1	0
1			DIRA			DIRB	DIRC

	Read/Write
DIRA	Direction of Port A 1 = input 0 = output
DIRB	Direction of Port B
DIRC	Direction of Port C

NOTE: Only mode 0 is currently supported, therefore the mode selection bits have been excluded.

On reset all ports are set to input.

2) Bit Set / Clear Format (Bit 7 = 0)
Writing to the control register using this format will set or clear the selected bit on the selected ports.

7	6	5	4	3	2	1	0
0	PC	PB	PA	SEL			SET

	Read/Write
SET	Set/Clear bit 1 = Set 0 = Clear
SEL	Bit Select 000 = Bit 0 001 = Bit 1 010 = Bit 2 011 = Bit 3 100 = Bit 4 101 = Bit 5 110 = Bit 6 111 = Bit 7
PA	1 = Modify Port A
PB	1 = Modify Port B
PC	1 = Modify Port C

8255 Port I/O Register

When the direction of the port is set to output, writing to this register will drive the associated pins. Reading from this register will return the current state of the pins, regardless of direction setting.

7	6	5	4	3	2	1	0
DATA							

	Read/Write	
DATA	Output bits	Input bits

8254 Control Register

There are three different formats used when writing to the control register: 1) Control Word Format, 2) Counter Latch Command Format and 3) Read-back Command Format.

1) Control Word Format
Writing this format sets the read/write format, mode and counting format of the selected counter. If SC = 11, a Read Back Command Format is being used.

7	6	5	4	3	2	1	0
SC		RW		M			BCD

	Read/Write
SC	Select Counter: 00 = Counter 0 01 = Counter 1 10 = Counter 2 11 = see Read Back Command
RW	Read / Write: 00 = see Counter Latch Command 01 = Read/Write LSB 10 = Read/Write MSB 11 = Read/Write LSB & MSB
M	Mode Selection: 000 = Mode 0 001 = Mode 1 X10 = Mode 2 X11 = Mode 3 100 = Mode 4 101 = Mode 5
BCD	Counting type: 0 = Binary 1 = BCD in 4 Decades

2) Counter Latch Command Format
Writing this format instructs the selected counter to latch the current count. The latched count is read on the next read to the counter register.

7	6	5	4	3	2	1	0
SC		0	0				

	Write
SC	Select Counter: 00 = Counter 0 01 = Counter 1 10 = Counter 2 11 = Read Back Command

3) Read-back Command Format
Writing this format instructs the counter selected counters (all can be selected at once) to latch the current status and/or the current count. When reading from the counter register the latched status is returned first, then the latched count.

7	6	5	4	3	2	1	0
1	1	CNT	STAT	SEL2	SEL1	SEL0	

	Write
CNT	0 = Latch count
STAT	0 = Latch status
SEL2	1 = Select Counter 2
SEL1	1 = Select Counter 1
SEL0	1 = Select Counter 0

8254 Counter Register

Writing to this register will supply the initial count to load or re-load into the counter. When reading from this register, the running count, latched count or latch status will be returned depending on commands issued to the control register.

1) Count Format
When read, the latched count or current count may be returned to depending on previously issued commands.

7	6	5	4	3	2	1	0
CNT							

	Write	Read
CNT	Counter load Value	Current Count Latched Count

2) Status Format
The status format is only read when the read-back command is issued with the read status selected.

7	6	5	4	3	2	1	0
OUT	NULL	RW		M			BCD

	Read
OUT	Current status of output pin
NULL	Indicates if the last count written to has been loaded 1 = Load pending 0 = Count loaded.
RW	Read/Write value written to control register
M	Mode value written to control register
BCD	Count type value written to control register

Counter Clock Source

This register allows the counter/timers to be clocked from internal timing resources rather than to the external clock signal.

7	6	5	4	3	2	1	0
	TC1_2	TC1_1	TC1_0		TC0_2	TC0_1	TC0_0

	Read/Write
TC0_0	Counter/Timer 0, Counter 0 1 = Internal, FPGA Clock / 4 0 = External Clock
TC0_1	Counter/Timer 0, Counter 1 1 = Internal, FPGA Clock / 8 0 = External Clock
TC0_2	Counter/Timer 0, Counter 2 1 = Internal, FPGA Clock / 16 0 = External Clock
TC1_0	Counter/Timer 1, Counter 0 1 = Internal, FPGA Clock / 4 0 = External Clock
TC1_1	Counter/Timer 1, Counter 1 1 = Internal, FPGA Clock / 8 0 = External Clock
TC1_2	Counter/Timer 1, Counter 2 1 = Internal, FPGA Clock / 16 0 = External Clock

User LED Register

This register controls the 4 LEDS D2-D5.

7	6	5	4	3	2	1	0
				LED3	LED2	LED1	LED0

	Read/Write
LED0	LED D2 0 = Off 1 = On
LED1	LED D3 0 = Off 1 = On
LED2	LED D4 0 = Off 1 = On
LED3	LED D5 0 = Off 1 = On

Revision Register

Reading this register will return the revision of the currently loaded FPGA configuration.

7	6	5	4	3	2	1	0
REV							

	Read
REV	Revision of FPGA configuration

Software Installation

The FreeForm/104 ships with a CD containing drivers for various operating systems and a SDK (software development kit) to help quickly develop digital I/O and counter/timer applications. Refer to the CD for instructions on how to install the drivers and SDK.

For other operating systems, please check the Connect Tech website's download zone:

http://www.connecttech.com/asp/Support/DownloadZone.asp

Specifications

Operating Environment

- Storage Temperature: -65°C to 150°C
- Operating Temperature: 0°C to 70°C (commercial)
  -40°C to 85°C (industrial)

Power Requirements

- +5VDC
- 0.75 W (0.150A @ 5V), average with standard reference design
- 2.75 W (0.550A @ 5V), maximum with all I/O toggling @ 10 Mbps
- Current requirements are design dependant.

PC/104 Bus Interface

- Standard configuration provides base address selection through a rotary switch
- PC/104 signals connected to the FPGA:

Control:	RESET, AEN, IOW, IOR
Address Data:	SD<7:0>, SA<11:0>
IRQ:	IRQ3, IRQ4, IRQ5, IRQ6, IRQ7, IRQ9, IRQ10, IRQ11, IRQ12, IRQ14, IRQ15
DMA:	DRQ0, DACK0, DRQ1, DACK1, DRQ2, DACK2, DRQ3, DACK3, TC

I/O Interfaces

- Programmable I/O: 96 pins 5V CMOS / TLL @ +/- 24 mA
- Fixed I/O: 18 pins 5V TTL @ +/- 12 mA

Dimensions

- Length: 9.58 cm (3.775 inches)
- Width: 9.00 cm (3.55 inches)
  * excludes I/O headers

Compliant to PC/104 specification 2.3

Weight

- 78 grams